TCNJ Mentored Undergraduate Summer Experience Program 2008 Proposal

COVER PAGE

Name:	**Orlando J. Hernandez**
Title:	**Assistant Professor**
Number of Years at TCNJ:	**3 years and 5 months**
Department:	**Electrical and Computer Engineering**
Contact Information:	**x2470, hernande@tcnj.edu**

Title of Research Program:	**Algorithms and High Performance Implementations of Image Compression, and Graphical Software Development Infrastructure**

Number of Student Collaborators: 2

Project and Learning Plan

These two research projects aim at the implementation of algorithms, and related architectures for image compression, and the development of a graphical software development infrastructure that will make it easier to implement embedded applications, such as image compression, in embedded processors. The aims of the specific projects are such that they yield publishable results in appropriate peer reviewed journals and/or academic professional conferences. Students will be co-authors with the faculty in these publications. Another goal of this program is that students continue their work or a part of it in Independent Study courses, Senior Capstone Design experiences, or graduate school after their graduation from TCNJ. Students will be working with the faculty in the School of Engineering's Image Processing and Understanding Laboratory. The faculty has received a grant from the National Science Foundation to implement this laboratory over the 04-06 academic years. This lab will be uniquely suited for these proposed research projects. The laboratory infrastructure consists of multiprocessor computer workstations, storage server and backup, nano-image acquisition and reproduction equipment, and computer-hosted Digital Signal Processing rapid prototyping boards; all connected over a high speed gigabit network with wireless capabilities. All the supporting professional software tools and uninterruptible power supplies complete this equipment infrastructure.

Several factors have determined the selection of a successful student to participate in this our program. Students were selected based on demonstrated enthusiasm and interest during an interview session by the faculty, and having a cumulative GPA of 3.0 or better. Additionally, the faculty mentored the students through putting together a resume to highlight their capabilities.

Although the faculty will be intricately involved with the work being done by the students in a full-time basis, the faculty-students team will hold formal attainment review meetings once a week. In these meetings the students will formally present the progress made on their assignments during that week, their plans for the following week, and any major challenges that they are facing. Additionally, during these meeting the faculty will present theory that is pertinent to the research, and guidance to the student on how to follow a rigorous research methodology flow. These topics include: literature research, state of the art determination, preliminary plans and hypotheses formulation, design of experiments, results evaluation, and results dissemination.

One part of this research project, executed by student Graham Apgar, will address the development of a new very large scale integration (VLSI) architecture for image compression. The proposed architecture will be designed to enable the compression of large sized images at video rates, and aid in the transmission and storage of video data, which is a fundamental goal and function of computer vision systems. To the applicant's knowledge, this is the first VLSI architecture for the new Windows Media Photo (WMP) image format put forth by Microsoft Corporation. Students will work with the faculty prototyping the architecture using a Xilinx Field Programmable Gate Array (FPGA) development environment, and appropriate hardware development platform.

The other part of this research project, executed by student Theodore Moskalenko, will address the development of a graphical software development infrastructure for embedded systems that can be used to implement image compression algorithms in embedded processors. This infrastructure will be based on the well-known engineering instrumentation tool LabView from National Instruments. This infrastructure, however, will not be limited to image compression. It could also be used in other embedded systems, such as robotics, design, control, and test applications, including critical testing in designing airplanes, environmental monitoring to preserve priceless manuscripts, and automating processes to make ice cream. By incorporating their own creativity, design, logic, and problem-solving skills, users will be able to explore endless engineering opportunities.

APPENDICES

FACULTY VITAE

PAST SURP AWARDS REPORT

BUDGET

STUDENTS APPLICATIONS

CURRICULUM VITAE

Orlando J. Hernandez, Ph.D.
PO Box 7718
Ewing, NJ 08628
+1 (609) 771-2470
E-Mail: hernande@tcnj.edu

Highlights:

- Teaching: VLSI Design, Digital Circuits and Microprocessors, Digital Image Processing, Computer Architecture & Organization.
- Experience with academic research in the areas of VLSI, image processing, and computer vision.
- Experience with guiding fourteen students in nine undergraduate student research projects in the areas of computer vision and related VLSI architectures with peer refereed published results.
- Experience with business management, program management, and chipset development - design and software integration at a system level.
- Experience with large team leadership and team work at a world wide level.
- Reviewer for the Fuzzy Sets and Systems Journal, Elsevier Science B.V.
- Reviewer for the IEEE Transactions on Systems, Man and Cybernetics - Part B: Cybernetics, IEEE Systems, Man and Cybernetics Society
- Reviewer for the IEEE Transactions on Pattern Analysis and Machine Intelligence, IEEE Computer Society
- Reviewer for the IEEE Transactions on Information Theory, IEEE Information Theory Society
- Reviewer for "INNOVATIONS 2005: WORLD INNOVATIONS IN ENGINEERING EDUCATION AND RESEARCH", International Network for Engineering Education and Research
- Experience with embedded processors systems architecting.
- Experience with digital signal processing systems.
- Experience with development of highly integrated ASICs, high data bandwidth ASICs, and VLSI circuits for DSP.
- Experience with ASIC design using Verilog, VHDL, Synopsys family of tools, and back-end tools.
- Experience with C, C++, Unix software development utilities, and assembly language for generic processors and DSPs.
- Experience with MATLAB and Microsoft productivity tools.

Academic Appointments:

The College of New Jersey	Ewing, New Jersey
Assistant Professor - Elec. & Computer Eng.	As of August, 2003

Southern Methodist University Dallas, Texas
Guest Lecturer 08/01 to 08/03
Have been invited repeatedly as a guest lecturer for the Computer Vision course in the department of Electrical Engineering.

Education:

Southern Methodist University Dallas, Texas
Doctor of Philosophy in Electrical Engineering 05/2002
Minor: Statistics.
Area of Concentration: Image Processing and Computer Vision.
Dissertation Title: Color Image Retrieval Using Multispectral Random Field Texture Models and Color Content Features.

University of South Florida Tampa, Florida
Master of Science in Electrical Engineering 05/1993
Area of Concentration: Digital and Analog VLSI Design for Communications and Digital Signal Processing.

University of South Florida Tampa, Florida
Bachelor of Science in Electrical Engineering 12/1991
GRADUATED MAGNA CUM LAUDE

Awards:

GRANTS (PI)
Precision Stabilization of a Ball Joint Gimbaled Mirror
$ 24, 850 - 2007-2008 year
DSCI, US Navy STTR

Acquisition of Instrumentation Systems for Education and Research in Image Processing and Understanding
$ 93, 320 - 9/1/04 to 8/31/06
National Science Foundation

CourseMaker Studio authoring suite. e-learning development and delivery tool
$ 3, 995 - Spring 2005
Learn.com Inc.

TMS320C6701 Digital Signal Processor (DSP), and TMS320C6000 DSP Platform Code Composer Studio Development Tools and Software
$ 3, 679 - Spring 2005
Texas Instruments Inc.

Xilinx DSP and Embedded Systems Design Tools and Software
$ 6,864 - Spring 2005
Xilinx Inc.

Xilinx Field Programmable Gate Arrays (FPGAs) and Complex Programmable Logic Devices (CPLDs) Development Tools and Software
$ 3, 990 - Spring 2004
Xilinx Inc.

FELLOWSHIPS
Selected as a participant in the 2004 Excellence in Engineering Education Teaching Workshop at the US Military Academy in West Point, NY. Selection was competitive for commitment to excellence in education.
$ 2, 500 - Summer 2004

SOSA
The College of New Jersey
2007-2008 Academic Year
2006-2007 Academic Year
2005-2006 Academic Year

Publications: *A Low Cost Advanced Encryption Standard (AES) Co-Processor Implementation*
In Press - Journal of Computer Science and Technology
Annotation: Refereed journal. Orlando Hernandez is the primary author of this publication, with three co-authors, who are TCNJ students. Two of these students have graduated, and the third continued the research, and is graduating in 2007. This paper describes research done by the authors at The College of New Jersey in its entirety. The IEEE (Institute of Electrical and Electronics Engineers) Transactions on VLSI (Very Large Scale Integration) Systems is published as a monthly journal under the co-sponsorship of the IEEE Circuits and Systems Society, the IEEE Computer Society, and the IEEE Solid-State Circuits Society. Design and realization of microelectronic systems using VLSI/ULSI technologies require close collaboration among scientists and engineers in the fields of systems architecture, logic and circuit design, chips and wafer fabrication, packaging, testing and systems applications. Generation of specifications, design and verification must be performed at all abstraction levels, including the system, register-transfer, logic, circuit, transistor and process levels. To address this critical area through a common forum, the IEEE Transactions on VLSI Systems have been founded. The editorial board, consisting of international experts, invites original papers which emphasize and merit the novel systems integration aspects of microelectronic systems including interactions among systems design and partitioning, logic and memory design, digital and analog circuit design, layout synthesis, CAD tools, chips and wafer fabrication, testing and packaging, and systems level qualification. Thus, the coverage of these Transactions focuses on VLSI/ULSI microelectronic systems integration.

A Combined VLSI Architecture for Nonlinear Image Processing Filters
IEEE Southeast Conference 2006, March 31 - April 2, 2006, Memphis, Tennessee
Annotation: Refereed conference paper. Orlando Hernandez is the primary author of this publication with co-authors Tara Keohane and Julia Steponanko. This paper is based on research done by Orlando Hernandez at The College of New Jersey with the co-authors, who were senior undergraduate Electrical and Computer Engineering students at TCNJ during the 2005-2006 academic year. The IEEE Southeast Conference is a scholarly conference held every year, and sponsored by the IEEE.

A High Performance VLSI Architecture for the Histogram Peak-Climbing Data Clustering Algorithm
IEEE Transactions on Very Large Scale Integration (VLSI) Systems, Volume 14, Number 2, February 2006

A Classification Methodology for Color Textures Using Multispectral Random Field Mathematical Models
Mathematical and Computational Applications, Volume 11, Number 2, 2006

Face Recognition Using Multispectral Random Field Texture Models, Color Content, and Biometric Features
34th Applied Imagery Pattern Recognition Workshop, October 19-21, 2005, Washington, D.C.
Annotation: Refereed conference paper. Orlando Hernandez is the primary author of this publication with co-author Mitchell Kleiman. This paper is based on research done by Orlando Hernandez at The College of New Jersey with the co-author, who is a senior undergraduate Electrical / Computer Engineering student at TCNJ. The purpose of the Applied Imagery Pattern Recognition (AIPR) annual workshops is to bring together researchers from government, industry, and academia in an elegant setting conducive to technical interchange across a broad range of disciplines. The papers span a range from research to fielded systems and provide, to managers and developers alike, a broad vision of the applicability of image analysis technologies.

Taking Advantage of Low Enrollment Scheduled Courses for the Integration of Research and Teaching
35th ASEE/IEEE Frontiers in Education Conference, October 19-22, 2005, Indianapolis, Indiana
Annotation: Refereed conference. Orlando Hernandez is the sole author of this publication. The FIE Conference has a long tradition of disseminating innovations that improve computer science, engineering, and technology (CSET) education. FIE is a major annual international conference devoted to improvements in CSET education. It is a forum for sharing ideas, learning about new developments in CSET education, and interacting with colleagues.

Classification of Color Textures with Random Field Models and Neural Networks
Journal of Computer Science & Technology, Volume 5, Number 3, October 2005
Annotation: Refereed journal. Orlando Hernandez is the primary author of this publication with co-authors John Cook, Cynthia De Rama, Michael Griffin, and Michael McGovern. This paper is based on research done by Orlando Hernandez at The College of New Jersey with the co-authors, who were senior undergraduate Electrical and Computer Engineering students at TCNJ during the 2003-2004 academic year. The Journal of Computer Science and Technology (JCS&T) is a semiannual and peer-reviewed International Journal promoting dissemination of research and technological implementation experiences in the areas of Computer Science, Engineering, and Information Systems.

C++ Encapsulated Dynamic Runtime Power Control for Embedded Systems
IEEE Southeast Conference 2005, April 8-10, 2005, Fort Lauderdale, Florida
Annotation: Refereed conference paper. Orlando Hernandez is the primary author of this publication with co-authors Godfrey Dande and John Ofri. This paper is based on research done by Orlando Hernandez at The College of New Jersey with the co-authors, who were senior undergraduate Electrical and Computer Engineering students at TCNJ during the 2004-2005 academic year. The IEEE Southeast Conference is a scholarly conference held every year, and sponsored by the IEEE.

Low-Cost Advanced Encryption Standard (AES) VLSI Architecture: A Minimalist Bit-Serial Approach
IEEE Southeast Conference 2005, April 8-10, 2005, Fort Lauderdale, Florida
Annotation: Refereed conference paper. Orlando Hernandez is the primary author of this publication with co-authors Thomas Sodon and Michael Adel. This paper is based on research done by Orlando Hernandez at The College of New Jersey with the co-authors, who were senior undergraduate Electrical and Computer Engineering students at TCNJ during the 2004-2005 academic year. The IEEE Southeast Conference is a scholarly conference held every year, and sponsored by the IEEE.

High Performance VLSI Architecture for Data Clustering Targeted at Computer Vision
IEEE Southeast Conference 2005, April 8-10, 2005, Fort Lauderdale, Florida

Color Image Segmentation Using Multispectral Random Field Texture Model & Color Content Features
Journal of Computer Science & Technology, Volume 4, Number 3, October 2004

A Case Study on Teaching Design to Undergraduates: A Comprehensive First Course in VLSI Design
International Conference on Engineering Education 2004, October 16-21, 2004, Gainesville, Florida

An Image Retrieval System Using Multispectral Random Models, Color, and Geometric Features
33rd Applied Imagery Pattern Recognition Workshop, October 13-15, 2004, Washington, D.C.

Teaching Comprehensive Real World VLSI Design to Undergraduate Students
2004 National Conference: Integrating Practice into Engineering Education, October 3-5, 2004
University of Michigan-Dearborn, Dearborn, Michigan

Color Image Retrieval Using Multispectral Random Field Texture Model & Color Content Features
Pattern Recognition Journal, Volume 36, Issue 8, August 2003

Color Image Retrieval Using Multispectral Random Field Texture Models
IEEE Digital Signal Processing Workshop, October 15-18, 2000

Using MATLAB for Algorithm Development and Performance Analysis: A Coordinate Mapping for a Rapid Prototyping System
1993 MATLAB Conference, Proceedings, October 18-20, 1993

Rapid Prototyping Using Laser Restructuring VLSI Circuits
4th International Workshop on Rapid System Prototyping, Proceedings, June 28-30, 1993

Industry Experience:

Maxim Integrated Products, Inc. - uController Business Dallas, Texas
Technical Business Manager 07/02 to 08/03

- Responsible for product definition to architect single chip microcontroller and DSP systems with analog content, as well as formulating business plans for each development program.
- Responsible for the following end equipments: electricity metering, safety system such as CO detectors and O2 monitors, hearing aids, networked media appliances, and digital audio players.

Texas Instruments, Inc. - Imaging & Audio Group Dallas, Texas
Design & Development Director 04/00 to 07/02

- Managed a large team of engineers developing next generation Digital Imaging and Internet Audio DSP platforms. These designs contain DSP core and memory, microcontroller, co-processors, and peripherals. Data conversion, analog, and on-chip software are included in the system level integration as well (System-on-a-Chip).
- Drove full technology entitlement and very aggressive time to market and profitability cycle times.
- Drove chip set roadmap for the business unit.
- The group is divided in different functional sub-team: Systems/architecture/software, design, platform hardware, and product engineering.
- The group is divided in sub-teams across several regions of the world: US, Japan, and India.

Texas Instruments, Inc. - Imaging & Audio Group Dallas, Texas
Streaming Media Business Manager 05/01 to 11/01

- Managed a group chartered with developing and marketing chipsets for Streaming Media end equipments. This team has the responsibility of defining a common platform for audio and imaging; then promote its wide adoption by 3rd parties, system houses, and customers. Ultimately, responsibility for development, execution, and marketing of the product fall within this group as well.

Texas Instruments, Inc. - ASIC/SLI Development Dallas, Texas
Design Manager 05/97 to 04/00

- Integrated a single chip system for a hard disk drive that contained a micro-controller, memories (including embedded flash), and ASIC logic.
- Interfaced with the customer to architect the integrated system solution.
- Led a team of design engineers engaged in the design of micro-controllers for hard disk drives, and the integration of hard disk drive ASICs.

- Led a team of design engineers developing micro-controllers for embedded system applications. The team is also responsible for the chip level design of some of the embedded systems. These were System-on-a-Chip class designs.

Texas Instruments, Inc. - Telecom Systems Division Dallas, Texas
Digital Signal Processing Systems Engineer 01/97 to 05/97

- Designed, coded, and tested Digital Signal Processing software for telecommunications systems platforms for voice recognition and speech processing with the TI TMS320C30 digital signal processor.

Texas Instruments, Inc. - ASIC Product Development Dallas, Texas
Applications Engineer 05/93 to 01/97

- Prototyped multiple hard disk drive controller ASICs.
- Performed the role of Program Manager, and led the development team working on the data buffer ASICs for the UltraSPARC (TM) processor.
- Developed and delivered training on ASIC products and libraries.
- Participated in the definition and development of ASIC products and libraries.

Affiliations: Membership in the ACM, the IEEE, along with the IEEE Computer Society and the IEEE Signal Processing Society, the American Society for Engineering Education, the National Society of Professional Engineers, and the Society of Hispanic Professional Engineers.

Foreign Languages:

Spanish	Can read, write, and speak fluently.
Japanese	Rudimentary.

PAST SURP AWARDS REPORT

Over the past three summers (2005, 2006, and 2007), the faculty has participated in the Summer Undergraduate Research Program. During these programs, 8 students have been positively impacted by working on 4 distinct projects. Outcomes of these activities are provided below:

PROJECT: NON-LINEAR IMAGE PROCESSING FILTER ARCHITECTURE
PUBLICATION:
A Combined VLSI Architecture for Nonlinear Image Processing Filters
Orlando J. Hernandez, Tara Keohane, and Julia Steponanko
IEEE Southeast Conference 2006, March 31 - April 2, 2006, Memphis, Tennessee
Orlando J. Hernandez: Primary author.
Tara Keohane and Julia Steponanko: **Co-authors. TCNJ Students.**

PROJECT: FACE RECOGNITION
PUBLICATION:
Face Recognition Using Multispectral Random Field Texture Models, Color Content, and Biometric Features
Orlando J. Hernandez and Mitchell Kleiman
34th Applied Imagery Pattern Recognition Workshop, October 19-21, 2005, Washington, DC
Orlando J. Hernandez: Primary author.
Mitchell Kleiman: **Co-author. TCNJ Student.**

PROJECT: A High Performance VLSI Architecture for Markov Random Field Parameters

This research addressed the development of a new very large scale integration (VLSI) architecture to compute parameters of a Markov Random Field model. The proposed architecture will be designed to enable the extraction of texture features from large sized images at video rates, and aid in the segmentation of video data, which is fundamental goal and function of computer vision systems. To the applicant's knowledge, this is the first VLSI architecture for computing a Markov Random Field model. The architecture will also be prototyped using a Xilinx Field Programmable Gate Array (FPGA) development environment.

PROJECT: Parallelization of Texture Analysis to Improve Performance

This research addressed the investigation of the CPU time and power necessary to achieve the results of a single process as intensive as texture analysis on a single processor. Then the issues involved in the parallelization of these algorithms were investigated. Parallelization was used via the formation of tightly coupled processor clusters, loosely coupled processor clusters, and a combination of these, to distribute processing. CPU time and power were compared for both the non-parallel and the parallel approaches. The issues of overhead and efficiency of parallelization was also investigated, and the effects of these were examined in terms of achievable real speedup versus theoretical speedup. The time taken by a single process can be greatly reduced by splitting the amount of work among several processors and computers.

BUDGET

ITEM	NUMBER	AMOUNT
Students Stipend		
Graham Apgar	1	$2,500.00
Theodore Moskalenko	1	$2,500.00
Students Housing		
Graham Apgar	1	$1,252.00
Theodore Moskalenko	1	$1,252.00
Faculty Stipend		
Orlando J. Hernandez	1	$1,000.00
Research Supplies/Equipment	-	$0.00
TOTAL		**$8,504.00**

Mentored Undergraduate Summer Experience
Summer 2008 Student Application

Name: Graham Apgar
Major: Computer Engineering
Year: 3
Completed Course Credits: 88
Expected Graduation Date: Spring 2009
GPA – Cumulative: 3.85
GPA – In Major: 3.87
Request On-campus Housing: Yes

Statement:

Given the broad spectrum of electrical and computer engineering fields, the curricula of these programs at TCNJ are often only starting points for students. As I prepare to enter my fourth year at the college, I have begun to prioritize my interests based on what I have learned so far. At this stage in my college experience, I hope to use the resources available at the college engineering department to focus on my interest in computer architecture and hardware design.

My goal is to gain experience and skills in these areas beyond that which can be learned in a classroom. Due to the complexity of the software used in hardware design, it would be wise for me to devote my time to mastering it as much as possible with the help of experienced faculty. I hope to gain a deeper understanding of the design processes for digital hardware used in the industry by applying my current skills to a larger project. I would like to emerge from college with not just a degree, but also a specialized set of skills and knowledge that will help me transition into the work force and/or perform further research.

I believe my academic and work history, as well as my interest in the subject, qualify me to collaborate on this project. My interests have been met with previous success in courses involving high level programming and assembly languages, digital logic and design, circuits, electronics and microcontrollers. I have also worked as a web application programmer for the past two and a half years, developing large programs in small teams over periods of months. Most importantly, I tend to thrive on challenging projects related to computer science and engineering, and often go above and beyond requirements for learning purposes. This is an important opportunity for me to learn and contribute to a real engineering problem; to take advantage of the expertise of Dr. Hernandez and to contribute to his work.

Mentored Undergraduate Summer Experience
Summer 2008 Student Application

Name: Ted Moskalenko
Major: Computer Engineering
Year: 3
Completed Course Credits: 138
Expected Graduation Date: Spring 2009
GPA – Cumulative: 3.125
GPA – In Major: 3.65
Request On-campus Housing: No

Statement:

In the Spring semester of 2007, I transferred from the Mathematics department to the Computer Engineering department, and I am convinced that I have found my calling. I have always enjoyed working with computers, and discovering how things work. Fortunately, the Computer Engineering department focuses on exactly those topics. Being able to do the hands on experiments brings what students learn in the classroom into a real environment. MUSE will provide me with the chance to further my knowledge by providing a time and place to study topics I enjoy in more depth. Working with faculty on a project will also assist in discovering the concentration within engineering that interests me most. The time period for MUSE is ideal for completing a research project, since faculty will be available when necessary. Furthermore, the experience that I will gain will be a worthy achievement that will help me stand out in the future, when applying for a job or continuing to graduate school.

Since I have taken many computer, electrical, and general engineering courses, I will be well prepared for the MUSE project. Each of the courses will somehow help me contribute to the project, ranging from circuit design to computer programming. I have completed a variety of projects for each of my classes, many of which have real life applications. Most, if not all, of the project I have already completed will assist me in the MUSE project. I have taken a plethora of computer science courses, and have learned many languages in my engineering courses. The knowledge that I have obtained will contribute to the completion of the project.

Since I only recently joined the engineering department, I have not had the chance to work on a project or independent study with faculty. However, I did have the chance to do this within the math department, and found it an enriching intellectual experience. Thus, I would like to gain the same experience within the engineering department as well. MUSE would provide the perfect environment, and an excellent experience that I will have the chance to enjoy.

Thus far, I have taken 7 courses with Dr. Hernandez, ranging from embedded systems, programming, and circuit design. I have enjoyed each of these areas, and feel that I have gained much necessary knowledge that will help me with my career. However, the area that I have enjoyed the most is the programming side of engineering. Thus, working on the MUSE project will allow me to gain more knowledge and experience in this field.